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Bartling et al.

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(54) **DUAL-PORT POSITIVE LEVEL SENSITIVE DATA RETENTION LATCH**

(71) Applicant: **Texas Instruments Incorporated**, Dallas, TX (US)

(72) Inventors: **Steven Bartling**, Plano, TX (US); **Sudhanshu Khanna**, Richardson, TX (US)

(73) Assignee: **TEXAS INSTRUMENTS INCORPORATED**, Dallas, TX (US)

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Related U.S. Application Data

(60) Provisional application No. 61/863,177, filed on Aug. 7, 2013.

(51) **Int. Cl.**
H03K 3/356 (2006.01)
H03K 3/037 (2006.01)

(52) **U.S. Cl.**
CPC ***H03K 3/0375*** (2013.01)

(58) **Field of Classification Search**
USPC 327/201–203, 206, 208, 212, 214, 218
See application file for complete search history.

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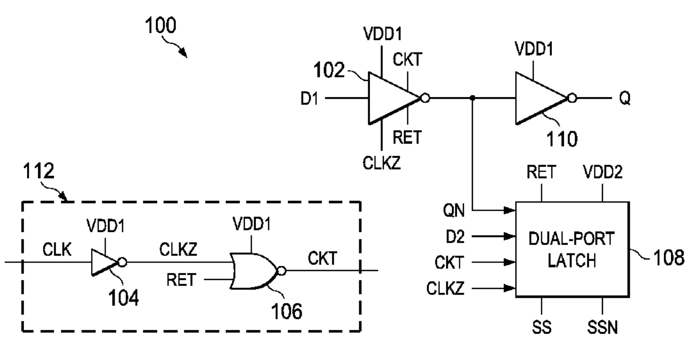
Primary Examiner — Hai L Nguyen

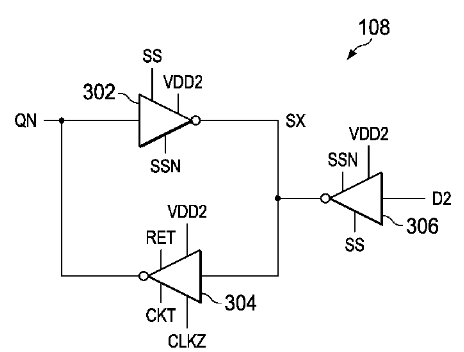
(74) *Attorney, Agent, or Firm* — John R. Pessetto; Charles A. Brill; Frank D. Cimino

(57) **ABSTRACT**

In an embodiment of the invention, a dual-port positive level sensitive data retention latch contains a clocked inverter and a dual-port latch. Data is clocked through the clocked inverter when clock signal (CKT) goes high, (CLKZ) goes low and retention control signal is low. The dual-port latch is configured to receive the output of the clocked inverter, a second data bit (D**2**), the clock signals (CKT) and (CLKN), the retain control signals (RET) and the control signals SS (SS) and (SSN). The signals (CKT), (CLKZ), (RET), (SS) and (SSN) determine whether the output of the clocked inverter or the second data bit (D**2**) is latched in the dual-port latch. Control signal (RET) determines when data is stored in the dual-port latch during retention mode.

7 Claims, 4 Drawing Sheets





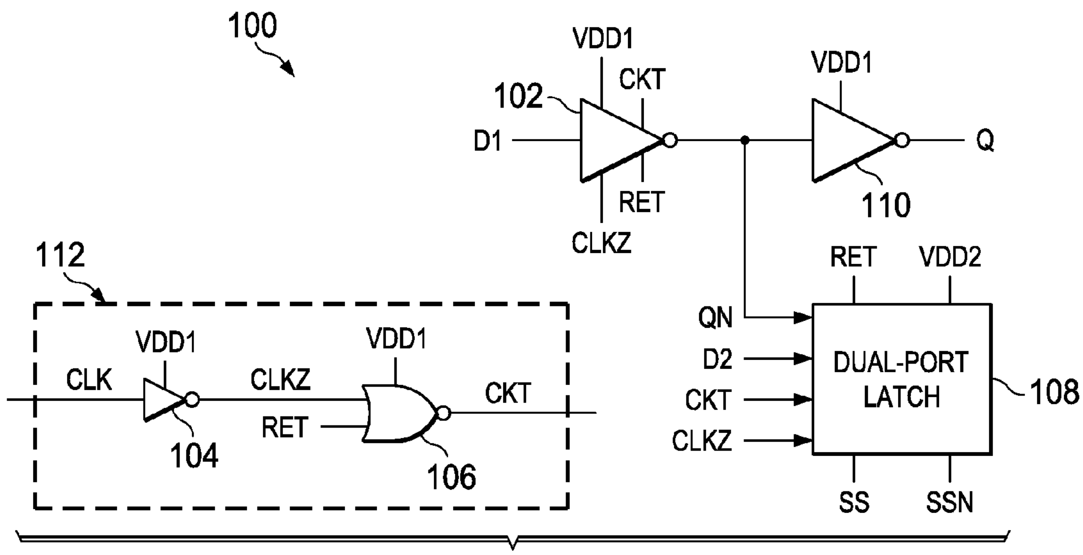


FIG. 1

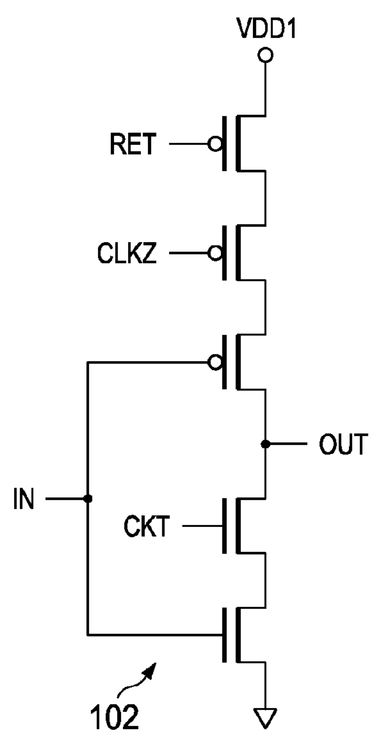


FIG. 2
(PRIOR ART)

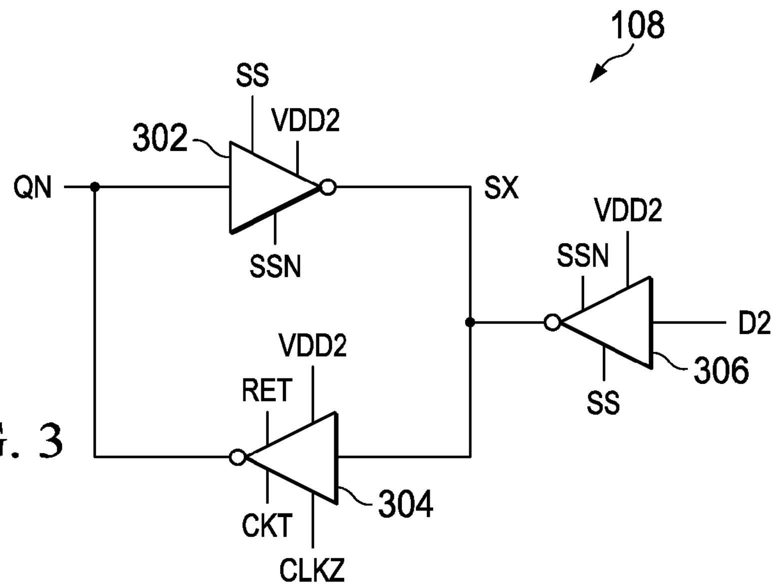


FIG. 3

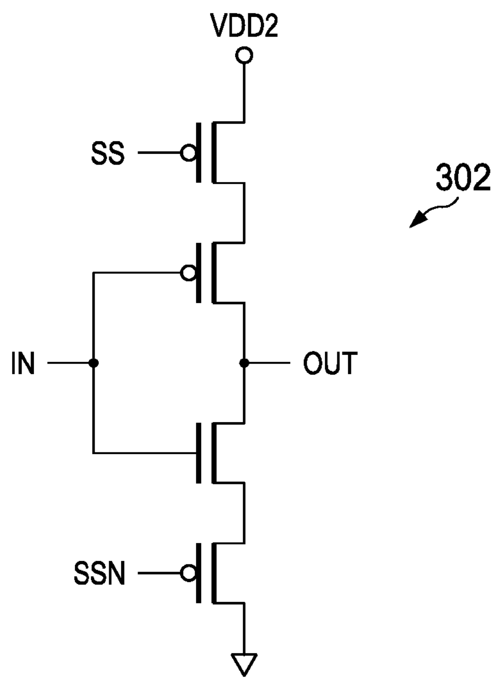


FIG. 4
(PRIOR ART)

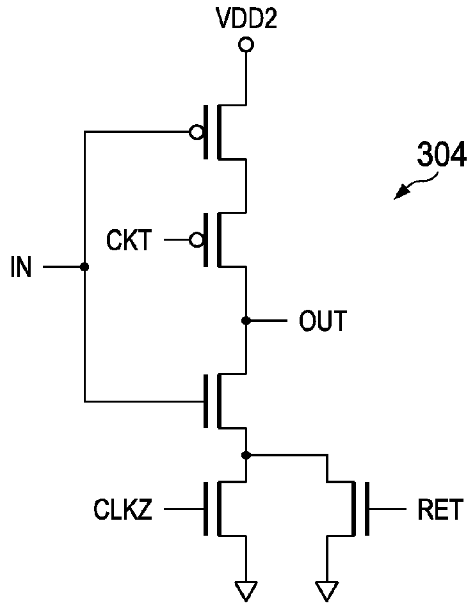


FIG. 5
(PRIOR ART)

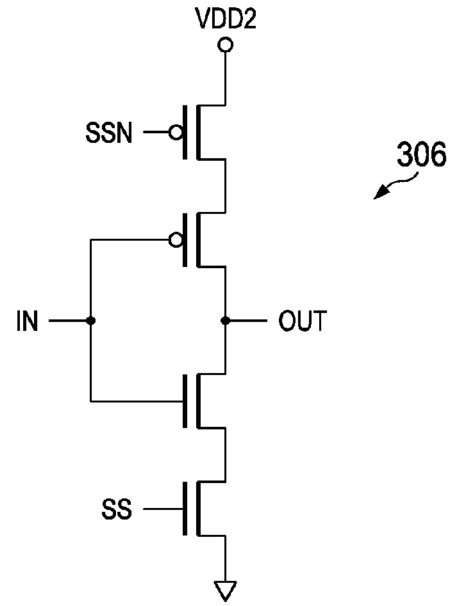


FIG. 6
(PRIOR ART)

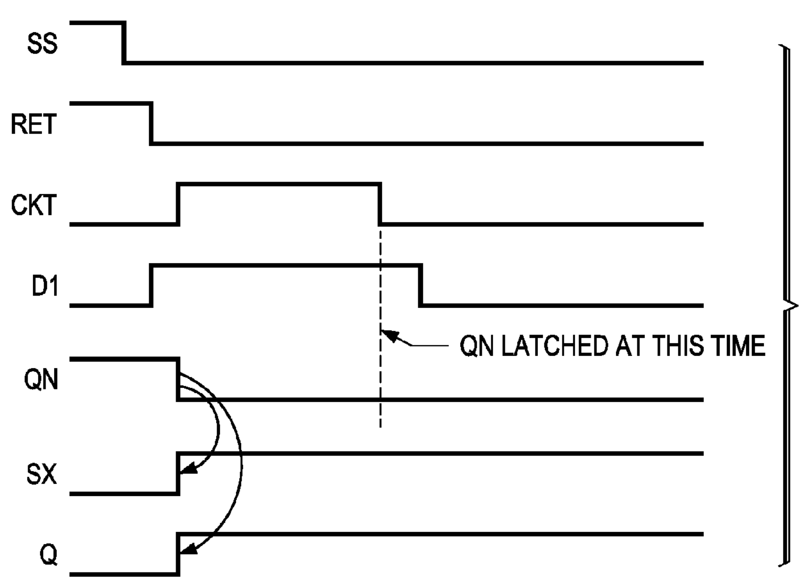


FIG. 7

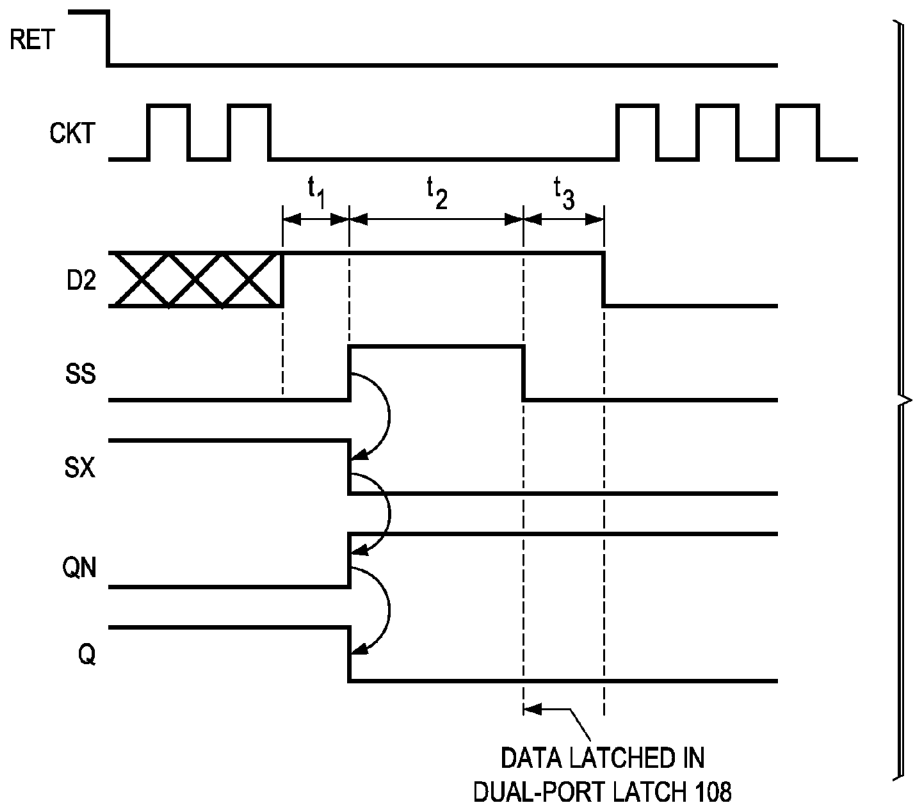

RET
CKT
t_1
t_2
t_3
D2
SS
SX
QN
Q
DATA LATCHED IN
DUAL-PORT LATCH 108

FIG. 8

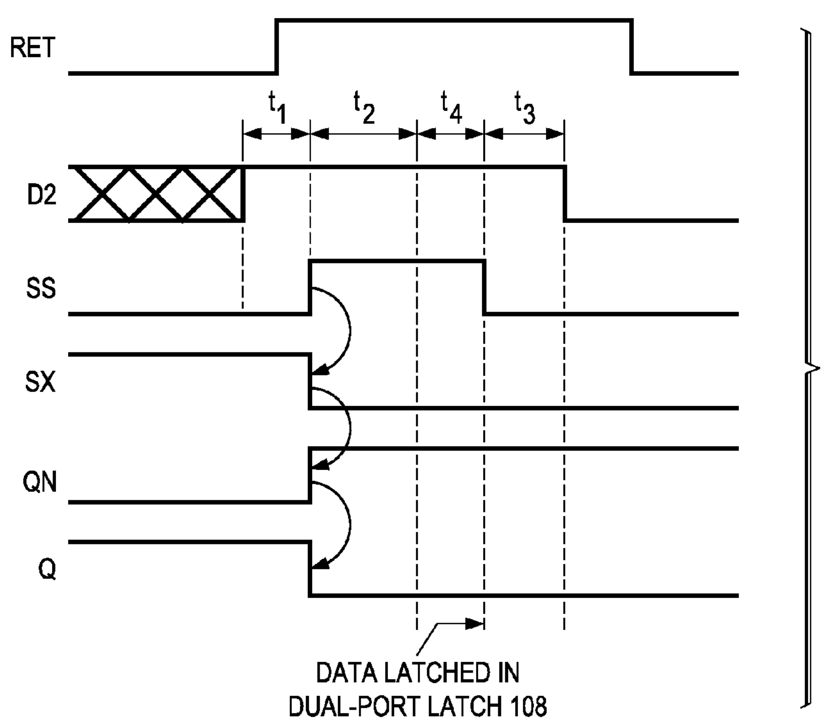

RET
t_1
t_2
t_4
t_3
D2
SS
SX
QN
Q
DATA LATCHED IN
DUAL-PORT LATCH 108

FIG. 9

DUAL-PORT POSITIVE LEVEL SENSITIVE DATA RETENTION LATCH

This application claims priority from Provisional Application No. 61/863,177, filed Aug. 7, 2013.

BACKGROUND

Several trends presently exist in the semiconductor and electronics industry. Devices are continually being made smaller, faster and requiring less power. One reason for these trends is that more personal devices are being fabricated that are relatively small and portable, thereby relying on a battery as theft primary supply. For example, cellular phones, personal computing devices, and personal sound systems are devices that are in great demand in the consumer market. It is also important that data on these devices be retained even when no power is supplied to the electronic device. Non-volatile memory circuits and non-volatile logic circuits are often used to meet these requirements.

Non-volatile logic implementation often requires updating sequential elements, such as latches, from a source external to the sequential element, such as a non-volatile memory. When non-volatile logic circuits are implemented to allow the updating of sequential elements, it is desired that the implementation of the non-volatile logic circuit does not significantly slow the operation of a sequential element.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a dual-port positive level sensitive data retention latch according to an embodiment of the invention.

FIG. **2** is a schematic diagram of a clocked inverter according to an embodiment of the invention. (Prior Art)

FIG. **3** is a schematic diagram of a dual-port latch according to an embodiment of the invention.

FIG. **4** is a schematic diagram of a tri-state inverter according to an embodiment of the invention. (Prior Art)

FIG. **5** is a schematic diagram of a clocked inverter according to an embodiment of the invention. (Prior Art)

FIG. **6** is a schematic diagram of a tri-state inverter according to an embodiment of the invention. (Prior Art)

FIG. **7** is a timing diagram showing signals SS, RET, D**1**, CLK, QN and the output of the latch Q according to an embodiment of the invention.

FIG. **8** is a timing diagram showing signals RET, CKT, D**2**, SS, SX, QN, and Q according to an embodiment of the invention.

FIG. **9** is a timing diagram showing signals RET, D**2**, SS, SX, QN, and Q according to an embodiment of the invention.

DETAILED DESCRIPTION

In an embodiment of the invention a dual-port positive level sensitive data retention latch **100** contains a clocked inverter **102**, an inverter **110**, a dual-port latch and a logic circuit **112** used to create internal clocks CLKZ and CKT from an external clock CLK. The clocked inverter **102** is configured to receive a first data bit D**1**, a retain control signal RET, and internal clock signals CLKZ and CKT. The dual-port latch **108** is configured to receive the output QN from the clocked inverter **102**, data input D**2**, clock signals CLKZ and CKT, the retain control signal RET and control signals SS and SSN. The signals CKT, CLKZ, RET, SS and SSN determine whether the output QN of the clocked inverter **102** or the second data bit D**2** is latched in the dual-port latch **108**.

Non-volatile logic implementations often require updating sequential elements (e.g. flip-flops) from an external source (e.g. non-volatile memory). In an embodiment of the invention, the dual-port latch includes **108** a second data input (port). The second data input is used to insert data from an external source. A tri-state inverter is added to the dual-port latch **108** to accommodate the second data input. This will be explained in more detail later in the specification. When external data needs to be inserted into the dual-port latch, the tri-state inverter is enabled. During this time, the latch feedback is disabled by causing a forward inverter to be tri-stated with the opposite control signal as the former tri-state inverter.

The circuitry used to add the second input to the dual-port latch **108** is not part of the critical timing path of the dual-port positive level sensitive data retention latch **100**. As a result, change to the regular performance of the dual-port positive level sensitive data retention latch **100** is negligible.

FIG. **1** is a block diagram of a dual-port positive level sensitive data retention latch **100** according to an embodiment of the invention. In a functional (i.e. normal) mode of operation, the retention mode signal RET is held at a logical low level, the control signal SS is held at a logical low level and the binary compliment signal SSN of the control signal SS is held a logical high level. Power is needed for functional mode operation so power supply VDD**1** and power supply VDD**2** are applied to the dual-port positive level sensitive data retention latch **100**.

FIG. **7** is a timing diagram showing data bit D**1**, clock signals CKT and CLKZ and the output Q of the dual-port positive level sensitive data retention latch **100** during the functional mode of operation. Because the RET is held at a logical low level, the binary logical compliment of D**1** is passed to the output QN when clock signal CKT transitions from a low to high logical value. FIG. **2** illustrates an embodiment of a clocked inverter **102**. QN is then presented to an input of the dual-port latch **108** and the inverter **110**. The output of inverter **110** drives the signal Q.

FIG. **3** is a schematic diagram of a dual-port latch **108** according to an embodiment of the invention. The dual-port latch **108** includes a first tri-state inverter **302** (see FIG. **4** for an embodiment of the first tri-state inverter **302**) with tri-state controls SS and SSN, a clocked inverter **304** (see FIG. **5** for an embodiment of the clocked inverter **304**) with control RET and a second tri-state inverter **306** (see FIG. **6** for an embodiment of the second tri-state inverter **306**) with tri-state controls SS and SSN.

When the dual-port positive level sensitive data retention latch **100** is operating in the functional mode and the clock signal CKT is at a high logic level, the tri-state inverter **302** is active and drives node SX of the dual-port latch **108** to the complimentary logical value of QN. When the clock signal CKT transitions from a high logical level to a low logical level, the logical level on the QN is latched by the clocked inverter **304**. In this embodiment of the invention, an inverter **110** is used to buffer QN. However, non-inverting buffers may be used as well. The tri-state inverter **306** is tri-stated in this mode because SS is a logical low level and SSN is a logical high level. As a result, D**2** is not transferred to node SX.

However, during another functional mode of operation, data D**2** may be written directly to the dual-port latch **108** (See FIG. **8**). During this functional mode, the clock signal CKT is held at a low logical level and CLKZ is held at a high logical level, RET is inactive (logical low value) with control signal SS held at a logical high level and control signal SSN held at logical low level. All other inputs to the dual-port latch **108** are don't-cares.

When control signal SS is held at a logical high level and control signal SSN is held at logical low level, tri-state inverter **306** is able to drive the complimentary value of D**2** onto node SX of the dual-port latch **108**. Because CKT and RET are held at logical low levels and CLKZ is held at logical high level, the clocked inverter **304** is active and drives node QN to the logical value of D**2**. The inverter **110** then inverts the logical value on node QN to its compliment. In this example, the compliment of D**2** is presented on node Q. Data signal D**2** must be held for the period t3 to insure that the correct value of D**2** is latched. Also, control signal SS must remain at logical high value for time t2 to insure that the correct value D**2** is latched.

When control signal SS is driven from a logical high level to a logical low level and SSN is driven from a logical low level to a logical high level, the tri-state inverter **306** is tri-stated and tri-state inverter **302** becomes active latching the logical value on node QN of the dual-port latch **108**.

The dual-port positive level sensitive data retention latch **100** can also be operated to retain data (RET mode) in the dual-port latch **108** (power supply VDD**2** is active) when clocked inverter **102**, logic circuit **112** and inverter **110** are powered off (i.e. power supply VDD**1** is inactivated). Because the dual-port positive level sensitive data retention latch **100** is being operated in the RET mode, the retention mode signal RET is held at a logical high level. Because power is not supplied to clocked inverter **102**, inverter **104**, NOR gate **106** and the inverter **110**, QN is not actively driven by clocked inverter **102**. In this manner, the data being retained in the dual-port latch **108** will not be inadvertently corrupted by the indeterminate output value of the clocked inverter **102** (the input is indeterminate as the supply VDD**1** is inactive or floating).

During retention mode of operation, data D**2** may be written directly to the dual-port latch **108**. During this retention mode, the control signal SS is driven to a logical high level following RET being driven to a logical high value (see FIG. **9**). The clock signals CKT and CLKZ are don't cares in this mode of operation in this embodiment. Before time t1, D**2** does not have to be driven to a logical level (i.e. D**2** may be a logical one, a logical zero, floating or tri-stated). D**2** must be driven to a logical one or a logical zero some time t1 before the control signal SS transitions from a logical zero to a logical one. D**2** must be stable for time t4 before the control signal SS transitions from a logical one to a logical zero and remain stable for time t3 afterwards in order to ensure D**2** will be correctly latched.

Because the control signal SS is driven to a logical high level following RET being driving to a logical high value, the tri-state inverter **302** is tri-stated and does not drive node SX of the dual-port latch **108**. Because the control signal SS is driven to a logical high and control signal SSN is driven to a logical low value, the tri-state inverter **506** is active and drives node SX to the complimentary value presented on D**2**. Because RET is a logical high value, the clocked inverter **504** is active and drives node QN. When the control signal SS returns to a logic low level and SSN returns to a logic high level, the value stored on node QN is latched between tri-state inverter **302** and clocked inverter **304** while tri-state inverter **306** is tri-stated. Data signal D**2** must be held for the period t3 to insure that the correct value of D**2** is latched. Also, control signal SS must remain at logical high value for time (t2+t4) to insure that the correct value D**2** is latched. Under this condition, the data written from D**2** remains latched in the dual-port latch **108** during retention mode.

The foregoing description has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and other modifications and variations may be possible in light of the above teachings. The embodiments were chosen and described in order to best explain the applicable principles and their practical application to thereby enable others skilled in the art to best utilize various embodiments and various modifications as are suited to the particular use contemplated. It is intended that the appended claims be construed to include other alternative embodiments except insofar as limited by the prior art.

What is claimed is:

1. A dual-port positive level sensitive data retention latch comprising:

a first clocked inverter configured to receive a first data bit (D**1**), a first clock signal (CKT), a second clock signal (CLKZ) and a retention mode control signal (RET) wherein the first clock signal (CKT), the second clock signal (CLKZ), and the retention mode control signal (RET) determine whether a data output (QN) from the first clocked inverter is the binary compliment of the first data bit (D**1**) or an indeterminate value;

a dual-port latch configured to receive the data output (QN) of the first clocked inverter, a second data bit (D**2**), the first clock signal (CKT), the second clock signal (CLKZ), the retention mode control signal (RET), a first latch control signal (SS) and a second latch control signal (SSN) wherein the first clock signal (CKT), the second clock signal (CLKZ), the retention mode control signal (RET), the first latch control signal (SS) and the second latch control signal (SSN) determine whether the data output (QN) of the first clocked inverter or the second data bit (D**2**) is latched in the dual-port latch;

wherein the dual-port latch comprises:

a first tri-state inverter, the first tri-state inverter having a data input, a first control input, a second control input and a data output wherein the data input of the first tri-state inverter is electrically connected to the data output (QN), the first control input of the first tri-state inventer is electrically connected to the first latch control signal (SS), and the second control input of the first tri-state inverter is connected to the second latch control signal (SSN);

a second tri-state inverter, the second tri-state inverter having a data input, a first control input, a second control input and a data output wherein the data input of the second tri-state inverter is electrically connected to the second data bit (D**2**), the first control input of the second tri-state inverter is electrically connected to the first latch control signal (SS), and the second control input of the second tri-state inverter is connected to the second latch control signal (SSN) and the outputs of the first and second tri-state inverters are electrically connected to each other;

a second clocked inverter, the second clocked inverter having a data input, a first control input, a second control input, a third control input and a data output wherein the data input of the second clocked inverter is electrically connected to the data outputs of the first and second tri-state inverters, the first control input of the second clocked inverter is electrically connected to the first clock signal (CKT), the second control input of the second clocked inverter is connected to the second clock signal (CLKZ), the third control input of the second clocked inverter is electrically connected to the retention mode control signal (RET), and the output of the second clocked inverter is electrically connected to the input of the first tri-state inverter.

2. The dual-port positive level sensitive data retention latch of claim 1 wherein the retention mode control signal (RET), a first latch control signal (SS) and a second latch control signal (SSN) are controlled external to the dual-port positive level sensitive data retention latch.

3. The dual-port positive level sensitive data retention latch of claim 1, further comprising a buffer wherein the buffer receives the data output (QN) and the buffer outputs the same logical value of the data output (QN).

4. The dual-port positive level sensitive data retention latch of claim 3 wherein the first clocked inverter and the buffer receive power from a first power supply (VDD1); wherein the dual-port latch receives power form a second power supply (VDD2).

5. The dual-port positive level sensitive data retention latch of claim 4 wherein the first power supply (VDD1) is turned off and the second power supply (VDD2) is turned on during operation of a retention mode; wherein power is only supplied to the dual-port latch.

6. A method of writing data into a dual-port latch of a dual-port positive level sensitive data retention latch in retention mode comprising;

disconnecting a first power supply (VDD1) from a clocked inverter configured to receive a first data bit (D1), a first clock signal (CKT), a second clock signal CLKZ and a retention mode control signal (RET) wherein the first clock signal (CKT), the second clock signal CLKZ and the retention mode control signal (RET) determine whether the data output (QN) from the clocked inverter is the binary compliment of the first data bit (D1) or an indeterminate value;

connecting a second power supply (VDD2) to the dual-port latch wherein the dual-port latch is configured to receive the data output (QN) of the clocked inverter, a second data bit (D2), the first clock signal (CKT), the second clock signal (CLKZ), the retention mode control signal (RET), a first latch control signal (SS) and a second latch control signal (SSN) wherein the first clock signal (CKT), the second clock signal (CLKZ), the retention mode control signal (RET), the first latch control signal (SS) and the second latch control signal (SSN) determine whether the data output (QN) of the clocked inverter or the second data bit (D2) is latched in the dual-port latch;

entering a retention mode by driving the retention mode control signal (RET) to a logical high value;

driving the second data bit (D2) to a binary logical level;

writing the second data bit (D2) into the dual-port latch by driving the first control signal (SS) to a logical high value and driving the second control signal (SSN) to a logical low value;

latching the second data bit (D2) into the dual-port latch by driving the first control signal (SS) to a logical low value and driving the second control signal (SSN) to a logical high value;

connecting the first power supply (VDD1) to the clocked inverter;

exiting the retention mode and entering a functional mode by driving the retention mode control signal (RET) to a logical low.

7. A method of writing data to a dual-port latch of a dual-port positive level sensitive data retention latch while in a functional mode comprising;

entering the functional mode by driving a retention mode control signal (RET) to a logical low value;

tri-stating an output of a clocked inverter by driving a first clock signal (CKT) to a logical low level and by driving a second clock signal (CLKZ) to a logical high level;

driving a second data bit (D2) of the dual port latch to a binary logical level wherein the dual-port latch is configured to receive the output of the clocked inverter, the second data bit (D2), the first clock signal (CKT), the second clock signal (CLKZ), the retention mode control signal (RET), a first control signal (SS) and a second control signal (SSN) wherein the first clock signal (CKT), the second clock signal (CLKZ), the retention mode control signal (RET), the first control signal (SS) and the second control signal (SSN) determine whether the data output (QN) of the clocked inverter or the second data bit (D2) is latched in the dual-port latch;

writing the second data bit (D2) into the dual-port latch by driving the first control signal (SS) to a logical high value and driving the second control signal (SSN) to a logical low value;

latching the second data bit (D2) into the dual-port latch by driving the first control signal (SS) to a logical low value and driving the second control signal (SSN) to a logical high value;

allowing the first (CKT) and second (CLKZ) clock signals to toggle.

* * * * *